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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,350	03/01/2002	Donald H. McNeil	303-01	3072

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PAUL AND PAUL
2900 TWO THOUSAND MARKET STREET
PHILADELPHIA, PA 19103

EXAMINER	
MASON, DONNA K	
ART UNIT	**PAPER NUMBER**
2111	5

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,350	MCNEIL, DONALD H.	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☒ Claim(s) *5 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because of undue length. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

It is unclear whether the external host bus 28, as recited on page 16, line 10 refers to the same or a different external host bus 29, as recited on page 16, line 25. Applicant is advised to review the disclosure to correct any discrepancies and make any corresponding changes to the drawings (*e.g.*, Figs. 1 and 2), where appropriate.

Appropriate correction is required. See 37 CFR 1.71.

Claim Objections

4. Claims 5 and 22 are objected to because of the following informalities:

Claim 5 recites, "control software . . . implement" in lines 1-2. Change "implement" to --implements--.

Claim 22 recites, "the element claim" in line 1. Insert --of-- between "element" and "claim".

Appropriate correction is required. See 37 CFR 1.75.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites the limitation "the RAM space" in line 14. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 1 recites the limitation "the MOTE" in line 16, wherein the dependent claims refer to either "the element" or the "elements". Applicant is asked to review the claims in their entirety, and use consistent terminology to refer to the same features.

9. Claim 3 recites the limitation "the elements" in line 1. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 3 recites the limitation " when physically combined in a sealed unit with a form factor meeting the prevailing standards for physical and electronic interfacing compatible with modular mass storage units" in lines 1-3. This limitation is unclear.

Claim 20 inherits the deficiencies of claim 3. *Because the interpretation of claims 3 and 20 would require considerable speculation, claims 3 and 20 have not been considered in view of the prior art.* (See *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962)).

11. Claim 4 recites the limitation "the elements" in line 1. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 4 recites the limitation " when physically combined in a sealed unit with a form factor meeting the prevailing standards for physical and electronic interfacing compatible with modular mass storage units" in lines 1-3. This limitation is unclear.

Because the interpretation of claim 4 would require considerable speculation, claim 4 has not been considered in view of the prior art. (See *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962)).

13. Regarding claim 5, the parenthetical term "logical" renders the claim indefinite because it is unclear whether this limitation is part of the claimed invention. See MPEP § 2173.05(d).

14. Claim 6 recites the limitation "a prevailing standard bus" in lines 1-2. It is unclear whether "a prevailing standard bus" as recited in claim 6 is the same as the prevailing standard bus previously recited in claim 1.

15. Claim 7 recites the limitation "the shared use" in line 2. There is insufficient antecedent basis for this limitation in the claim. This lack of antecedent basis renders claim 7 unclear.

Claims 8-14 inherit the deficiencies of claim 7. *Because the interpretation of claims 7-14 would require considerable speculation, claims 7-14 have not been considered in view of the prior art.* (See *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962)).

16. Claim 7 recites the limitation "the operating state" in line 2. There is insufficient antecedent basis for this limitation in the claim. (Applicant is reminded that "various operating states" was previously recited in claim 1.

17. Claim 10 recites the limitation "said non-volatile RAM storage" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. Applicant is advised to review all the claims, which depend from claim 10 to make changes in view of this rejection, where appropriate (*e.g.*, claim 11 recites "said non-volatile RAM storage").

18. Claim 10 recites the limitation "a virtual passive mass storage" in line 3. It is unclear whether "a virtual mass storage" as recited in claim 10 is the same or a different virtual mass storage as previously recited in claim 1.

19. Claim 11 recites "RAM storage" in line 2 (second occurrence). It is unclear whether this "RAM storage" refers to the same RAM storage as previously recited, for example, in claim 11 ("said non-volatile RAM storage).

20. Claim 12 recites "a soft lattice topology" in line 1. Does Applicant intend to recite --a software lattice topology--?

21. Claim 15 recites "a plurality of said topology elements" in lines 14-15. It is unclear whether this plurality of said topology elements refers to the same "a plurality of Modular Operating Topology Elements (MOTEs)" as previously recited in lines 2-3.

22. Claim 18 recites the limitation "said self-contained CPU and memory and operating system software and end-user application(s) " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

23. Claim 19 recites the limitation "said self-contained CPU and memory and operating system software and end-user application(s) " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

24. Claim 20 recites the limitation "said self-contained CPU and memory and operating system software and end-user application(s) " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

25. Claim 21 recites the limitation "said self-contained CPU and memory and operating system software and end-user application(s) " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

26. Claim 22 recites the limitation "said self-contained CPU and memory and operating system software and end-user application(s) " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

27. Claim 23 recites the limitation "said self-contained CPU and memory and operating system software and end-user application(s) " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

28. Claim 24 recites the limitation "said self-contained CPU and memory and operating system software and end-user application(s) " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

29. Applicant is advised to carefully review all of the claims for any additional 35 USC 112, second paragraph problems, and to make corrections as where appropriate.

30. Claims 2, 8, 9, 13, 16, and 17 inherit the deficiencies of their respective base claims.

Double Patenting

31. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

32. Claims 1-14 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-14 of copending Application No. 10/224,920. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

33. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

34. Claims 15-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-24 of copending Application No. 10/224,920, respectively.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the examined claims 15-24 are generic to the modular operating topology element (MOTE) of copending Application No. 10/224,920, and claims 15-24 of copending Application No. 10/224,920 fall entirely within the scope of the examined claims 15-24.

More specifically, because the MOTE of claims 15-24 of copending Application No. 10/224,920 is a species of the generic category defined by the MOTE of the examined claims 15-24, the MOTE of the examined claims 15-24 is anticipated by the MOTE of copending Application No. 10/224,920.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claims 1, 2, 18, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,675,761 to Paul, et al. ("Paul") in view of U.S. Patent No. 5,943,297 to Baker, and further in view of U.S. Patent No. 6,490,646 to Leydier.

With regard to claim 1, Paul discloses a modular operating topology element (MOTE), including: a central processing unit (CPU) (Fig. 2, item 62); an internal hardware bus (Fig. 2, item 60) connected to said central processing unit; a non-volatile RAM (Fig. 2, item 72) connected to said hardware bus and accessible by said CPU; a non-volatile ROM (Fig. 2, item 70) connected to said hardware bus and accessible by said CPU; an interrupt control module (Fig. 2, item 78) connected to said hardware bus and operating as an interrupt monitor for prompting various operating states of said CPU; and a host bus I/O module (Fig. 2, item 102) for connecting said internal hardware bus to a prevailing standard host external bus; wherein the RAM space is managed by said CPU as workspace memory and as a virtual passive mass storage as seen by the host external bus under interrupt-driven multiprogramming within the MOTE.

With regard to claim 2, Paul discloses the MOTE, further including a peripheral device I/O module for interconnecting optional peripheral devices to said internal hardware bus (Fig. 2, items 88, 86, 82, 84, and 80).

Paul does not expressly disclose a battery-backed real time clock-calendar unit connected to the hardware bus for providing time and date information to said CPU, as recited in claim 1.

Baker discloses a battery-backed real time clock-clock calendar unit that can be connected to a hardware bus for providing time and date information to the CPU (*see generally*, Fig. 2).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Baker with Paul. The suggestion or motivation for doing so would have been to track the hours, minutes, seconds, day, month, and year for the system and user (column 1, lines 17-29).

Therefore, it would have been obvious to combine Baker with Paul.

With regard to claims 1, 18, 19, and 21, Paul in view of Baker does not expressly disclose where the element is within a miniaturized package, as recited in claim 1. Paul in view of Baker further does not expressly disclose all the features of claims 18, 19, and 21.

With regard to claims 1, 18, 19, and 21, Leydier discloses where an element is within a miniaturized package; where an element serves as a means for partitioning functionality and for reducing the computing load for attached host equipment; where an element serves as a means for packaging, distributing, and storing proprietary software and computing services with minimal exposure to illegal copying, tampering, software piracy, and other misuse; and where an element serves as a means to isolate its self-

contained functionality from changes in host hardware, host operating systems, and other software in attached host equipment and to provide said functionality in highly compatible hot-pluggable and physically dismountable physical and electronic packaging ready for use with only minimal installation procedures. (See *generally*, Fig. 3 and column 1, lines 11-15; and column 2, lines 51-57).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Leydier with Paul in view of Baker. The suggestion or motivation for doing so would have been to provide a means for storing and processing confidential data in a secure manner (column 1, lines 11-15).

Therefore, it would have been obvious to combine Leydier with Paul in view of Baker to obtain the invention as specified in claims 1, 2, 18, 19, and 21.

37. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul in view of Baker, further in view of Leydier as applied to claim 1 above, and further in view of U.S. Patent No. 6,205,532 to Carvey, et al. ("Carvey").

With regard to claims 5 and 6, Paul in view of Baker, further in view of Leydier discloses where control software is resident in the ROM and RAM (*see* Paul, column 3, lines 35-43); and where the element is capable of connection to a prevailing standard external bus for acting as an extended mass storage volume to host equipment connected to said external bus (*see* Paul, Fig. 2, item 102).

With regard to claims 5 and 6, Paul in view of Baker, further in view of Leydier does not expressly disclose a non-hierarchical lattice topology of parallel and concurrent

logical processes on a software (logical) bus for partitioning the functions running on said CPU and for managing logical priority queues of messages for said logical processes, as recited in claim 5.

Carvey discloses a non-hierarchical lattice topology of parallel and concurrent logical processes on a software (logical) bus for partitioning the functions running on the CPU and for managing logical priority queues of messages for the logical processes, as recited in claim 5 (*see, e.g.*, Fig. 1).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Carvey with Paul in view of Baker, further in view of Leydier. The suggestion or motivation for doing so would have been to provide a means to incrementally expand the topology of a multi-module system by connecting the modules in a configuration, and changing the configuration remotely (column 1, lines 63-66).

Therefore, it would have been obvious to combine Carvey with Paul in view of Baker, further in view of Leydier to obtain the invention as specified in claims 5 and 6.

38. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul in view of Baker, and further in view of Carvey.

With regard to claim 15, Paul discloses an element containing a central processing unit (Fig. 2, item 62) and [an] internal hardware bus (Fig. 2, item 60), a non-volatile RAM (Fig. 2, item 72) connected to said internal hardware bus and accessible under the exclusive control of said CPU, a non-volatile ROM (Fig. 2, item 68) connected

to said internal hardware bus and accessible exclusively by said CPU, an interrupt control module (Fig. 2, item 78) connected to said internal hardware bus and providing status signals to said CPU, and one or more optional peripheral I/O interfaces providing access to said internal hardware bus (Fig. 2, items 80, 82, 84, 88, and 86), where the interrupt control module operates with the CPU to independently control the ultra-concurrent and ultra-modular logical processing of operations within each said topology element, and where the CPU controls the access to the RAM to project virtual passive mass storage to said I/O connection; where a plurality of the topology elements are each programmed with a specific logical queue address for receiving logical messages and to perform a specific system support or end-user application function including the management of internally stored data.

Paul does not expressly disclose a battery-backed real time clock-calendar unit connected to the internal hardware bus and providing time and date information to the CPU, as recited in claim 15.

Baker discloses a battery-backed real time clock-calendar unit connected to the internal hardware bus and providing time and date information to the CPU, as recited in claim 15 (*see generally*, Fig. 2).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Baker with Paul. The suggestion or motivation for doing so would have been to track the hours, minutes, seconds, day, month, and year for the system and user (column 1, lines 17-29).

Therefore, it would have been obvious to combine Baker with Paul.

With regard to claims 15-17, Paul in view of Baker does not disclose a connection network forming a software lattice topology for the operation of identical computing elements in connection with host equipment, including: a plurality of Modular Operating Topology Elements (MOTEs); where any of the topology elements may be selectively programmed to be operative and non-operative to reconfigure and rescale said soft-latticed network; and where the reconfiguration includes reprogramming individual element computing functions.

With regard to claims 15-17, Carvey discloses a connection network forming a software lattice topology for the operation of identical computing elements in connection with host equipment, including: a plurality of Modular Operating Topology Elements (MOTEs); where any of the topology elements may be selectively programmed to be operative and non-operative to reconfigure and rescale said soft-latticed network; and where the reconfiguration includes reprogramming individual element computing functions (*see generally*, Fig. 1 and column 1, lines 45-67 to column 3, lines 1-63).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Carvey with Paul in view of Baker.

The suggestion or motivation for doing so would have been to provide a means to incrementally expand the topology of a multi-module system by connecting the modules in a configuration, and changing the configuration remotely (column 1, lines 63-66).

Therefore, it would have been obvious to combine Carvey with Paul in view of Baker to obtain the invention as specified in claims 15-17.

39. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul in view of Baker, further in view of Carvey as applied to claim 15 above, and further in view of Leydier.

Paul in view of Baker, further in view of Carvey discloses all the features of independent claim 15. Paul in view of Baker, further in view of Carvey does not expressly disclose all the features of dependent claims 22-24.

With regard to claims 22-24, Leydier discloses the network where the modular operating topology element serves as a means for partitioning functionality and for reducing the computing load for attached host equipment; where the modular operating topology element (MOTE) serves as a means for packaging, distributing, and storing proprietary software and computing services with minimal exposure to illegal copying, tampering, software-piracy, and other misuse; and where the modular operating topology element serves as a means to isolate its self-contained functionality from changes in host hardware, host operating systems, and other software in attached host equipment and to provide the functionality in highly compatible hot pluggable and physically dismountable physical and electronic packaging ready for use with only minimal installation procedures. (*See generally*, Fig. 3 and column 1, lines 11-15; and column 2, lines 51-57).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Leydier with Paul in view of Baker, further in view of Carvey.

The suggestion or motivation for doing so would have been to provide a means for storing and processing confidential data in a secure manner (column 1, lines 11-15).

Therefore, it would have been obvious to combine Leydier with Paul in view of Baker, further in view of Carvey to obtain the invention as specified in claims 22-24.

Conclusion

40. A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM

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